

LISTING OF CLAIMS:

1. (Currently Amended) A serial communication transceiver comprising:
 - a trapezoidal wave signal generation circuit for producing a trapezoidal wave signal responsive to a control signal, wherein the trapezoidal wave signal generation circuit includes means for decreasing harmonic components in the trapezoidal wave signal and for suppressing noise superimposed on the trapezoidal wave signal;
 - a driver circuit for delivering the trapezoidal wave signal to a communication line; and
 - a receiver circuit for receiving [[the]] another trapezoidal wave signal over the communication line, wherein the receiver circuit includes:
 - a waveform shaping circuit for shaping the another trapezoidal wave signal ~~waveform~~ received over the [[LIN bus]] communication line to thereby logically bi-level the signal into two logical levels; and
 - a filter circuit for receiving the logically bi-leveled signal and for releasing a resultant 2-level signal, wherein the filter circuit has a filtering time at the rise of the logically bi-leveled signal substantially equal to a filtering time at the fall of the logically bi-leveled signal.
2. (Original) A serial communication transceiver according to claim 1, wherein the means for decreasing harmonic components in the trapezoidal wave signal and for suppressing noise superimposed on the trapezoidal wave signal comprises:
 - a first current output circuit for conducting a charge current to a capacitor that generate the trapezoidal wave signal;

a second current output circuit for conducting a discharge current from the capacitor responsive to the control signal, wherein the discharge current is approximately twice the value of the charge current;

a first threshold voltage generation circuit for producing a plurality of first threshold voltages by basing a reference on a first power supply line of a power supply voltage;

a second threshold voltage generation circuit for producing a plurality of second threshold voltages by basing a reference on a second power supply line of the power supply voltage; and

a current control circuit for controlling the first and second current output circuits based on a capacitor voltage with the first and second threshold voltages such that the voltage difference between the capacitor voltage and a voltage of the first or second power supply lines corresponds to the charge and discharge currents of the capacitor.

3. (Original) A serial communication transceiver according to claim 1, wherein the filter circuit further comprises:

a current mirror circuit comprised of a first and second transistors having their control electrodes connected to each other, with the voltage of the joined control electrodes varying in response to the variation in level of the input signal;

a first constant current circuit connected to the first transistor;

a filtering capacitor;

a second constant current circuit for producing a constant current that is $1/N$ ($N>1$) of a constant current flowing through the second transistor connected in series to the filtering capacitor;

an offset voltage generation circuit connected between one terminal of the filtering capacitor to which the constant current from the second constant current circuit flows in, and the second transistor, wherein the offset voltage generation circuit is adapted to produce a prescribed offset voltage; and

a logical bi-leveling circuit for producing an output signal having two logical levels based on the voltage between terminals of the filtering capacitor.

4. (Original) A filter circuit for an input signal having two logical levels, the filter circuit comprising:

a current mirror circuit comprised of a first and second transistors having their control electrodes connected to each other, with the voltage of the joined control electrodes varying in response to the variation in level of the input signal;

a first constant current circuit connected to the first transistor;

a filtering capacitor;

a second constant current circuit which produces a constant current which is $1/N$ ($N>1$) of a constant current flowing through the second transistor which is connected in series to the filtering capacitor;

an offset voltage generation circuit which is connected between one terminal of the filtering capacitor on which the constant current from the second constant current circuit flows in and the second transistor, and adapted to produce a prescribed offset voltage; and

a logical bi-leveling circuit for producing an output signal having two logical levels based on the voltage between the terminals of the filtering capacitor.

5. (Original) A filter circuit according to claim 4, wherein the offset voltage generation circuit produces an off set voltage which is equal to the voltage variation width on the joined control electrodes of the transistors which is derived from the voltage variation of the input signal.

6. (Original) A filter circuit according to claim 5, wherein the offset voltage generation circuit comprises a transistor of the same type as the first transistor, with the base and collector or the gate and drain of the offset voltage generating transistor being connected to each other.

7. (Currently Amended) A filter circuit according to claim 6, wherein the logical bi-leveling circuit comprises a comparison circuit for comparing the voltage of one terminal of the filtering capacitor with a threshold voltage by basing the reference voltage on another terminal of the filtering capacitor, wherein the comparison circuit has a first threshold voltage used when the voltage across the filtering capacitor is rising and a second threshold voltage used when the capacitor voltage is falling, wherein the first threshold voltage being set equal to a differential

voltage ~~bet-ween~~ between a full-charge voltage of the filtering capacitor and the second threshold voltage.

8. (Original) A filter circuit according to claim 5, wherein the logical bi-leveling circuit comprises a comparison circuit for comparing the voltage of one terminal of the filtering capacitor with a threshold voltage by basing the reference voltage on another terminal of the filtering capacitor, wherein the comparison circuit has a first threshold voltage used when the voltage across the filtering capacitor is rising and a second threshold voltage used when the capacitor voltage is falling, wherein the first threshold voltage being set equal to a differential voltage between a full-charge voltage of the filtering capacitor and the second threshold voltage.

9. (Original) A filter circuit according to claim 4, wherein the logical bi-leveling circuit comprises a comparison circuit for comparing the voltage of one terminal of the filtering capacitor with a threshold voltage by basing the reference voltage on another terminal of the filtering capacitor, wherein the comparison circuit has a first threshold voltage used when the voltage across the filtering capacitor is rising and a second threshold voltage used when the capacitor voltage is falling, wherein the first threshold voltage being set equal to a differential voltage between a full-charge voltage of the filtering capacitor and the second threshold voltage.

10. (Original) A filter circuit according to claim 4, wherein the second constant current circuit produces a constant current that is a half of a constant current flowing through the second transistor.

11. (Currently Amended) A filter circuit according to claim 10, wherein the filter circuit is implemented within ~~[[a-n]]~~ an asynchronous serial communication receiver comprising a waveform shaping circuit which reforms the signal waveform of asynchronous serial communication data, which is sent over a communication line, into a signal waveform having two logical levels, wherein the filter circuit is adapted to receive the data signal with a reformed waveform, and wherein a reception register holds the output data signal of the filter circuit.

12. (Original) A filter circuit according to claim 11, wherein the asynchronous serial communication receiver is used for a vehicle on-board communication network based on a Local Interconnect Network (LIN) scheme.

13. (Original) A trapezoidal wave signal generation circuit comprising:

- a capacitor having one terminal connected to a first power supply line and another terminal adapted to generate a trapezoidal wave signal;
- a first current output circuit connected between a second power supply line and the another terminal of the capacitor, wherein the first current output circuit is for conducting a charge current to the capacitor;
- a second current output circuit for conducting a discharge current that is twice the charge current, wherein the second current output circuit conducts the discharge current from the capacitor when a waveform control signal is at a first level, and halts the current conduction when the waveform control signal is at a second level;

a first threshold voltage generation circuit for producing a plurality of threshold voltages by basing a reference on a voltage of the first power supply line;

a second threshold voltage generation circuit for producing a plurality of threshold voltages by basing another reference on a voltage of the second power supply line; and

a current control circuit for controlling the first and second current output circuits based on a comparison of the voltage between the terminals of the capacitor with the threshold voltages such that a voltage difference between the capacitor terminal voltage and the voltage of the first or second power supply line corresponds to the charge and discharge currents of the capacitor.

14. (Original) A trapezoidal wave signal generation circuit according to claim 13, wherein the current control circuit increases or decreases the charge and discharge currents at an increment or decrement of a certain reference current each time the capacitor terminal voltage exceeds any of the threshold voltages.

15. (Original) A trapezoidal wave signal generation circuit according to claim 13, wherein the first and second threshold voltage generation circuits produce threshold voltages that are symmetric across a center voltage of the voltages of the first and second power supply lines.

16. (Original) A trapezoidal wave signal generation circuit according to any of claim 13, wherein the first and second threshold voltage generation circuits are each comprised of a plurality of diodes and a constant current circuit connected in series between the first and second power supply lines.

17. (Original) A trapezoidal wave signal generation circuit according to claim 16, wherein the first threshold voltage generation circuit produces three threshold voltages that are different in steps by the amount of the forward voltage VF of pn junction by basing the reference on the voltage of the first power supply line, and the second threshold voltage generation circuit produces three threshold voltages that are different in steps by the forward voltage VF by basing the another reference on the voltage of the second power supply line.

18. (Original) A trapezoidal wave signal generation circuit according to claim 16, wherein the waveform generation circuit is adapted to receive a 2-level transmission data signal to be used as the waveform control signal and wherein a driver circuit receives the trapezoidal wave signal and outputs the trapezoidal wave signal over a communication line.

19. (Original) A trapezoidal wave signal generation circuit according to claim 18, being implemented within an asynchronous serial communication transmitter.

20. (Original) A trapezoidal wave signal generation circuit according to claim 18, wherein the asynchronous serial communication transmitter is used for a vehicle on-board communication network based on the Local Interconnect Network (LIN).